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EXAMINER	
KIM, DAVID S	

ART UNIT	PAPER NUMBER
2613	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,605	HARTZELL ET AL.	
	Examiner	Art Unit	
	DAVID S. KIM	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Applicant's response to the objection to **claims 8 and 14** in the previous Office Action (mailed on 03 July 2008) is noted and appreciated. Applicant responded by amending the claims. Applicant's response overcomes the previous objection, which is presently withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. **Claims 1, 3-8, and 11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Arvanitakis et al. (U.S. Patent No. 5,005,939, hereinafter "Arvanitakis") in view of Ramaswami et al. (*Optical Networks: A Practical Perspective, 2nd ed.*, hereinafter "Ramaswami"), Phillips (U.S. Patent No. 5,565,675), Nourrcier, Jr. et al. (U.S. Patent No. 5,696,657, hereinafter "Nourrcier"), Nakanishi et al. (U.S. Patent No. 7,136,594 B2, hereinafter "Nakanishi"), Block et al. (U.S. Patent No. 5,039,194, hereinafter "Block"), and Chou et al. (U.S. Patent Application Publication No. 2002/0140081 A1, hereinafter "Chou").

Regarding claim 1, Arvanitakis discloses:

A transceiver system, comprising:

a transmitter portion (e.g., circuitized section 61 for transmitter 31 in Fig. 1) arranged on a bottom layer (1st layer in Fig. 1 would be on the "bottom" if viewed upside-down) of a multi-layer printed circuit board (e.g., printed circuit board 15 in Fig. 1; 15 is shown to be multilayered in Fig. 5 and col. 8, l. 13), the transmitter portion capable of providing signals to a transmitter optical subassembly configured to transmit optical signals from the transceiver system (e.g., the transmitter elements for transmitter 31 in Fig. 1, wherein the transmitter elements are configured to transmit optical signals);

a receiver portion (e.g., circuitized section 63 for receiver 33 in Fig. 1) arranged on the bottom 1st layer in Fig. 1 would be on the "bottom" if viewed upside-down) layer of the multi-layer printed circuit board (e.g., printed circuit board 15 in Fig. 1; 15 is shown to be multilayered in Fig. 5 and col. 8, l. 13), the receiver portion capable of receiving signals from a receiver optical subassembly configured to receive optical signals into the transceiver system (e.g., the receiver elements for receiver 33 in Fig. 1, wherein the receiver elements are configured to receive optical signals).

Arvanitakis does not expressly disclose:

a ***high-voltage power supply*** arranged on a ***top*** layer of the multi-layer printed circuit board, the high-voltage power supply providing a ***bias voltage*** for the receiver optical sub assembly; and

a ***metallic ground plane*** arranged on a first intermediate layer of the multi-layer printed circuit board between the top layer and the bottom layer, the metallic ground plane providing ***electrical shielding*** between the high-voltage power supply and the transmitter portion and the receiver portion.

Regarding the limitation of a ***power supply***, notice that one would obviously implement some kind of power supply for the various components of the apparatus of Arvanitakis, as suggested by the "power pin" teaching in col. 8, l. 9-13).

Regarding the limitation of a ***high-voltage*** power supply, notice that Arvanitakis broadly discloses the use of a photodiode, noting that several are known in the art (col. 6, l. 7). There are several types of photodiodes, as exemplified by the pin photodiodes and avalanche photodiodes (APD) of Ramaswami (p. 195-197). At the time the invention was made, it would have been obvious to one of ordinary skill in the

art to employ either of these types of photodiodes, such as an APD. One of ordinary skill in the art would have been motivated to do this since Arvanitakis broadly discloses the use of a photodiode and Ramaswami provides further helpful detail on particular types of photodiodes to actually implement. Also, in the case of an APD, it provides a comparative benefit over other types of photodiodes by having a greater responsitivity than other types of receiver elements (Ramaswami, p. 197, 1st full paragraph). An APD generally requires a ***high-voltage power supply for bias voltage***, so an obvious variation of Arvanitakis with an APD would also employ a ***high-voltage power supply for bias voltage***.

Regarding the limitations of arranging a power supply on a ***top*** layer of a multi-layer printed circuit board, i.e., arranging the ***high-voltage power supply for bias voltage*** on the side of the board **opposite** from the side with the receiver (and transmitter) portion, notice teachings from Phillips, Nourrcier, and Nakanishi.

First of all, the ***location*** of the high-voltage power supply for bias voltage should be determined. The teachings of Phillips and Nourrcier provide a suitable location: receiver and bias supply in close proximity, i.e., on the **same board** (Phillips, detector U6 and bias voltage circuit on the same printed wiring board 13 in Figs. 1-2; Nourrcier shows that bias voltage circuit components Q1-Q4 of Phillips do correspond to an APD bias circuit (Qb1-Qb4 of APD bias circuit 311 in Fig. 1 of Nourrcier), as noted by Phillips, col. 3, l. 30-40). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to employ such a location in the prior art of record. One of ordinary skill in the art would have been motivated to do this since Arvanitakis is relatively silent about the location of the high-voltage power supply for bias voltage, and Phillips and Nourrcier speak into this silence with further details for a suitable location: receiver portion and high-voltage power supply for bias voltage on the **same board**.

Additionally, Nakanishi provides a further modification for arranging the location of circuitry relative to other circuitry: allocating mainly optoelectronic elements to one surface of a circuit board and electronic or electric elements to the **opposite** surface of the circuit board (e.g., col. 4, l. 7-10). In the environment of the prior art of record, this arrangement would correspond to arranging electronic or electric elements, e.g., the ***high-voltage power supply for bias***

voltage, on the surface of the board **opposite** from optoelectronic elements, e.g., 31 and 33 of Fig. 1 of Arvanitakis, which would also be **opposite** from the surface with the transmitter and receiver portions of Arvanitakis (61 and 63 in Fig. 1). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to employ such an arrangement. One of ordinary skill in the art would have been motivated to do this to provide extra space for other elements, such as other electronic or electric elements (Nakanishi, col. 4, l. 10-12), or to provide size-reduction and cost-reduction (Nakanishi, Figs. 10-11, col. 10, l. 42-53).

Regarding the limitations of the ***ground plane***, and the ***electrical shielding***, notice that the practice of locating circuitry on opposite sides of a multi-layer circuit board with a ground plane in between the circuitry on opposite sides of the board is known in the art, as shown by Block (Fig. 5, "internal…grounds planes be provided, which inherently provide electrical isolation between the components mounted on the top and bottom surfaces of the card" in col. 10, l. 65-68). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement these internal ground plane teachings in the multi-layer printed circuit board of the prior art of record (the result would be the arrangement of the power supply and the transmitter and receiver portions on opposite sides of the multi-layer printed circuit board (power supply on the ***top*** layer) with a ground plane between the power supply and other circuitry. One of ordinary skill in the art would have been motivated to do this since doing so would prevent electromagnetic interference (Chou, abstract). Moreover, notice that ground planes are known to be metallic (Chou, paragraph [0053]).

Regarding claim 3, Arvanitakis in view of the references applied above (hereinafter the "RAA") does not expressly disclose:

(claim 3) The system according to claim 1, wherein a second intermediate layer of the multi-layer printed circuit board having vias is arranged between the first intermediate layer and the top layer.

(claim 4) The system according to claim 3, wherein a third intermediate layer of the multi-layer printed circuit board having vias is arranged between the first intermediate layer and the bottom layer.

(claim 5) The system according to claim 4, wherein an interconnect layer is arranged between the first intermediate layer and the third intermediate layer.

However, Arvanitakis does disclose the use of multiple layers (Arvanitakis, multilayered board in Fig. 5 and col. 8, l. 13), and the use of vias for connecting multiple layers (Arvanitakis, holes for pins 69 in the multilayered board in Fig. 5). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include any of these various layers and vias to provide obvious variants of the system of Arvanitakis in view of the RAA. One of ordinary skill in the art would have been motivated to do this for any variety of suitable reasons, e.g., addition of components and circuitry.

Regarding claim 6, Arvanitakis in view of the RAA does not expressly disclose:

The system according to claim 1, further including a microcontroller system arranged on the top layer and the bottom layer.

However, the use of a microcontroller system for a system, such the system of Arvanitakis in view of the RAA, is an extremely well known practice in the art. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to place a microcontroller system on the top and bottom layers. One of ordinary skill in the art would have been motivated to do this to locate microcontroller components in close proximity of the circuits that they would control, such as the power supply of the top layer and the transmitter and receiver portions of the bottom layer.

Regarding claims 7 and 8, claims 7 and 8 are claims that introduce limitations that correspond to the limitations all introduced by claim 1. Therefore, the recited limitations in claim 1 read on the corresponding limitations in claims 7 and 8.

Regarding claim 11, Arvanitakis in view of the RAA discloses:

The method of claim 8, further including arranging a second intermediate layer of the multi-stack printed circuit board between the top layer and the bottom layer (e.g., Arvanitakis, any suitable layer of the various layers of the multilayered board in Fig. 5), the second intermediate layer including vias to provide electrical contact with traces on the top layer (e.g., Arvanitakis, holes for pins 69 in the multilayered board in Fig. 5).

Regarding claims 12-13, Arvanitakis in view of the RAA does not expressly disclose:

(claim 12) The method of claim 11, further including arranging a third intermediate layer of the multi-stack printed circuit board between the first intermediate layer and the second intermediate layer, the third intermediate layer providing traces.

(claim 13) The method of claim 12, further including arranging a fourth intermediate layer of the multi-stack printed circuit board between the first intermediate layer and the bottom layer, the fourth intermediate layer including vias.

However, Arvanitakis does disclose the use of multiple layers (Arvanitakis, multilayered in Fig. 5 and col. 8, l. 13) and the use of vias for connecting multiple layers (Arvanitakis, holes for pins 69 in Fig. 5). Also, the use of traces is also well known for connecting circuitry. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include any of these various layers, vias, and traces to provide obvious variants of the system of Arvanitakis in view of the RAA. One of ordinary skill in the art would have been motivated to do this for any variety of suitable reasons, e.g., addition of components and circuitry.

Regarding claim 14, claim 14 is an apparatus claim that introduces limitations that correspond to the limitations introduced by system claim 1. Therefore, the recited means in apparatus claim 14 read on the corresponding means in system claim 1.

5. **Claims 2 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Arvanitakis in view of the RAA as applied to the claims above, and further in view of Nelson et al. (U.S. Patent No. 5,097,393, hereinafter “Nelson”).

Regarding claim 2, Arvanitakis in view of the RAA does not expressly disclose:

The system according to claim 1, wherein the transmitter portion and the receiver portion are arranged in a split-ground arrangement.

However, electrical circuitry generally requires a connection to ground. Instead of connecting the transmitter portion and the receiver portion to a common ground, split-ground arrangements are known in the art, as shown by Nelson (col. 12, l. 26-52). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include such an arrangement in the system of Arvanitakis in view of the RAA. One of ordinary skill in the art would have been motivated to do this to provide electrical

isolation (Nelson, col. 12, l. 27-28), which generally reduces electrical interference between various components. For example, one could provide electrical isolation between the transmitter portion and the receiver portion to reduce electrical interference between these portions by employing a split-ground arrangement instead of a common ground arrangement.

Regarding claim 10, Arvanitakis in view of the RAA does not expressly disclose:

The method of claim 8, further including providing a split ground between the high-voltage power supply and the other circuitry.

However, electrical circuitry generally requires a connection to ground. Instead of connecting the high-voltage power supply and the other circuitry to a common ground, split-ground arrangements are known in the art, as shown by Nelson (col. 12, l. 26-52). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include such an arrangement in the system of Arvanitakis in view of the RAA. One of ordinary skill in the art would have been motivated to do this to provide electrical isolation (Nelson, col. 12, l. 27-28), which generally reduces electrical interference between various components. For example, one could provide electrical isolation between the high-voltage power supply and the other circuitry to reduce electrical interference between these portions by employing a split-ground arrangement instead of a common ground arrangement.

Response to Arguments

6. Applicant's arguments with respect to the Claim Rejections Under 35 U.S.C. 103(a) (filed on 02 December 2008, REMARKS, p. 7-8) have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The references made of record and not relied upon are considered pertinent to applicant's disclosure.

Carden et al. (U.S. Patent No. 5,202,943) is cited to show a transceiver system similar to the one shown in Arvanitakis.

Ishizuka et al. (U.S. Patent No. 5,479,288) is cited to show the placement of a high voltage generating circuit for an APD (601 in Figs. 18-19) on the same printed circuit board (401 in Figs. 18-19) as circuitry for the APD (204 and 205 for light receiving module 202 in Fig. 12A).

Sawada et al. (U.S. Patent No. 5,742,480) is cited to show various multilayer printed circuit board structures (e.g., Figs. 4, 11, 12, 16, and 17) for an optical transceiver (e.g., Fig. 18).

Glenn (U.S. Patent No. 6,150,193) is cited to show the use of a floating ground plane as a shield (abstract).

Ames et al. (U.S. Patent No. 6,617,518 B2) is cited to show the placement of a transmitter portion and a receiver portion (34 in Fig. 1) on the same side of a printed circuit board (top side of 32 in Fig. 1)

Daikuhara et al. (U.S. Patent Application Publication No. 2008/0007930) is cited to show the placement of a transmitter portion and a receiver portion on one side of a multilayer printed circuit board (side (A) in Fig. 5) and a power supply on the opposite side of the board (power supply circuit 126 on side (B) in Fig. 5).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID S. KIM whose telephone number is (571)272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N. Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. S. K./
Examiner, Art Unit 2613

/Kenneth N Vanderpuye/
Supervisory Patent Examiner, Art Unit 2613